UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,130	03/01/2004	David C. Newbury	H0782	2638

22898 7590 09/28/2005

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,130	NEWBURY ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-7, 10-13, 16-17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cowan (6605951).

Regarding claim 1, Cowan disclose [see Figs. 1 and 3] a method for failure analysis of small contacts in integrated circuits (IC die 22), comprising: providing a plurality of opposing electrical contacts (bump contacts 62); and configuring the electrical contacts (62) to contact a sample (die 22) in an offset pattern such that any one electrical contact may contact more than one conductor in the sample and any opposing electrical contact (62) is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact.

Regarding claim 2, Cowan disclose configuring the contacts (62) to be offset in two perpendicular lateral directions [via interconnectors 11 and 20 see Fig. 3].

Regarding claim 3, Cowan disclose the respective offsets in the two perpendicular lateral directions [via interconnectors 11 and 20] are unequal and vary from contact to contact.

Regarding claim 6, Cowan discloses [see Figs. 1 and 3] a method for failure analysis of small contacts in integrated circuits (IC die 22), comprising: providing a plurality of opposing electrical contact arrays (bump contacts 62); and configuring the electrical contact arrays (62) to

contact a sample (22) in a pattern that is offset in two perpendicular lateral directions [via interconnectors 11 and 20] such that any one electrical contact in one of the contact arrays (62) may contact more than one conductor in the sample and any opposing electrical contact in an opposing contact array is offset- positioned to contact no more than one of the conductors contacted by the one electrical contact (62).

Regarding claim 7, Cowan discloses the respective offsets in the two perpendicular lateral directions [via interconnectors 11 and 20] are unequal and vary from contact to contact.

Regarding claim 10, Cowan discloses using the electrical contact arrays (62) for at least one of: periodically testing integrated circuits (22) during fabrication; and identifying at least one of the manufacturing equipment and the integrated circuits (22) present in an operating manufacturing process.

Regarding claim 11, Cowan disclose [see Figs. 1 and 3] a tester (tester 18) for failure analysis of small contacts in integrated circuits (IC die 22), comprising: a plurality of opposing electrical contacts (bump contacts 62); and means (interconnectors 11 and 20) for configuring the electrical contacts (62) to contact a sample in an offset pattern such that any one electrical contact (62) may contact more than one conductor in the sample (22) and any opposing electrical contact (62) is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact (62).

Regarding claim 12, Cowan disclose the contacts (62) are offset in two perpendicular lateral directions [via interconnector 11 and 20].

Regarding claim 13, Cowan disclose the respective offsets in the two perpendicular lateral directions [via interconnectors 11 and 20] are unequal and vary from contact to contact.

Regarding claim 16, Cowan disclose a tester (tester 18) for failure analysis of small contacts in integrated circuits (IC die 22), comprising: a plurality of opposing electrical contact arrays (bump contacts 62); and means (interconnectors 11 and 20) for configuring the electrical contact arrays (62) to contact a sample (22) in a pattern that is offset in two perpendicular lateral directions such that any one electrical contact (62) in one of the contact arrays may contact more than one conductor in the sample and any opposing electrical contact (62) in an opposing contact array is offset-positioned to contact no more than one of the conductors contacted by the one electrical contact (62).

Regarding claim 17, Cowan disclose the respective offsets in the two perpendicular lateral directions [via interconnectors 11 and 20] are unequal and vary from contact to contact.

Regarding claim 20, Cowan discloses using the electrical contact arrays (62) for at least one of: periodically testing integrated circuits (22) during fabrication; and identifying at least one of the manufacturing equipment and the integrated circuits (22) present in an operating manufacturing process.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 4-5, 8-9, 14-15 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowan (6605951) in view of Takao (6639417).

Regarding claims 4, 8, 14 and 18, Cowan disclose a tester (tester 18) for failure analysis of small contacts in integrated circuits (IC die 22), comprising: a plurality of opposing electrical contact arrays (bump contacts 62). However, he does not disclose a parametric test structure as claimed. Takao discloses [Fig. 6] a tester (tester 3) for failure analysis of small contacts in integrated circuits (IC wafer 2), comprising: a plurality of opposing electrical contact arrays (wafer prober 5) and a parametric test structure (parametric testing system 1) for testing the opposing contacts. Further, Takao teaches that the addition of parametric testing system is advantageous because it test wafers in the process for manufacturing semiconductor circuit devices. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cowan by adding parametric test structure as taught by Takao in order to test wafers in the process for manufacturing semiconductor circuit devices.

Regarding claims 5, 9, 15 and 19, Cowan disclose a tester (tester 18) for failure analysis of small contacts in integrated circuits (IC die 22), comprising: a plurality of opposing electrical contact arrays (bump contacts 62). However, he does not disclose means for using the parametric test structure as claimed. Takao discloses [Fig. 6] a tester (tester 3) for failure analysis of small

contacts in integrated circuits (IC wafer 2), comprising: a plurality of opposing electrical contact arrays (wafer prober 5), a parametric test structure (parametric testing system 1) for testing the opposing contacts and means (computer 6A) for using the parametric test structure (1) to adjust the offset pattern of the contacts (5). Further, Takao teaches that the addition of means for using parametric testing system is advantageous because it test wafers in the process for manufacturing semiconductor circuit devices and controls the tester while processing measured data. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cowan by adding parametric test structure as taught by Takao in order to test wafers in the process for manufacturing semiconductor circuit devices and controls the tester while processing measured data.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see cited references on PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
September 26, 2005